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Design and measurement of signal processing system for cavity beam position monitor

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Abstract In this paper, in order to achieve the output signal processing of cavity beam position monitor (CBPM), we develop a digital intermediate frequency receiver architecture based signal processing system, which consists of radio frequency (RF) front end and high speed data acquisition board. The beam position resolution in the CBPM signal processing system is superior to 1 μm. Two signal processing algorithms, fast Fourier transform (FFT) and digital down converter (DDC), are evaluated offline using MATLAB platform, and both can be used to achieve, the CW input signal, position resolutions of 0.31 μm and 0.10 μm at –16 dBm. The DDC algorithm for its good compatibility is downloaded into the FPGA to realize online measurement, reaching the position resolution of 0.49 μm due to truncation error. The whole system works well and the performance meets design target.

Key words Cavity beam position monitor, RF front end, Digital down converter, Fast Fourier transform, FPGA

1 Introduction

Cavity beam position monitor (CBPM) is very key for free electron laser (FEL) or linear collider (LC) facility because submicron or even nanometer position resolution is required when beam passes through long undulator section in FEL or arrives on target interaction point in LC[1,2]. Achieving the resolution of nanometer level, the CBPM is more potential than the electro-static strip-line BPMs.

Shanghai deep ultraviolet FEL (SDUV-FEL) facility is operated in the high gain harmonic generation, the scaled demonstrator system for Shanghai soft X-ray FEL project is being underway[3], and its beam position resolution should be superior to 1 μm according to the goal of CBPM signal processing system. A prototype CBPM with high quality factor has been installed on SDUV-FEL. Beam test based on wide bandwidth oscilloscope has been conducted[13], indicating that the CBPM outputs and its operational principle are useful to design signal processing system, but cannot reach optimal resolution of FEL or LC due to limitation of analog to digit converter (ADC). In the future, the appropriative digitizer would process the RF signals directly by ADC technique. So far, the RF signals must be downconverted by analog electronics before being digitized.

The heterodyne and homodyne methods are used for the radio techniques[4] and the conversion of the signal to a higher frequency. But they can deteriorate the system performance. In the heterodyne receiver, an additional filter in front of the mixer is applied to reject the image frequency, and the two-stage down-conversion makes the receiver full of more components, thus making against system integration. When the homodyne directly downconverted RF signal to baseband, the unbalance or mismatches in the in-phase/quadrature-phase (I/Q) channels would induce the error. Also, leakage from the local oscillator (LO) to the mixer RF port will introduce the interference to direct current.

However, the complex receiver design has been simplified with the advances in data converter and radio technology. The digitizer capabilities with a

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few hundreds of MHz and high precision can be available from the market.

In this paper, the digital receiver architecture[5] is applied to the RF front end in signal processing system. The RF signals are directly downconverted to a low intermediate frequency (IF), *I*/Q demodulation can be moved from analog to digital domain.

All the data converter process is implemented in a commercial data acquisition board ICS1554-002 (GE Corp.)[6], which has high precision 16-bit ADC up to 160 MSPS sample rate and Vertex 5 FPGA device. The pulse-by-pulse beam position in the single shot of many micropulses can be measured by digital signal processing algorithm.

2 System setup

The CBPM signal processing system consists of a dedicated RF front end and a commercial digitizer, the quality factor (Q), which is a key parameter for designing CBPM, is inversely proportional to the output signal intensity and bandwidth, and directly proportional to the decay time of output signal[7]. So the high/low Q needs different design methods to determine the RF front, we designed two prototypes of CBPM with high/low Q. The dedicated RF front end was developed to cover the two designs by changing the different IF low pass filters (LPF)[8].

The RF front end based on the RF receiver architecture is absolutely essential to convert the RF signals to IF. For CBPM with high/low Q, the IF and LPF selection are particularly critical. Table 1 shows the detail in our system design.

Table 1 Parameters of CBPMs and RF front end

	Prototype 1	Prototype 2
Resonant frequency	5.712 GHz	4.700 GHz
Loaded Q	~5600	~60
Signal intensity	Weak	Strong
Decay time	~156 ns	~2 ns
BPF Stop Band	Low	High
LNA Gain	High	Low
IF	20 MHz	20 MHz
Bandwidth	10–20 MHz	<10 MHz or less
Sample Rate	160 MHz	160 MHz
Algorithm	DDC or FFT	DDC

For the high quality factor, the signal bandwidth is narrow, but the signal intensity of the cavity output is low. So the high performance of RF front must be required to improve the intensity. Also there are enough samples processed by the digital signal process (DSP) algorithm to enhance the noise level in certain bandwidth. For the low quality factor, the intensity of CBPM output is particularly high and the bandwidth is very wide. The performance requirement for RF front end is lower than that of CBPM with high Q. The time constant of low Q CBPM output is small due to the direct proportion to Q. So there are no enough samples for FFT technique. Only the DDC algorithm works well for it.

2.1 RF front end

The RF signal of CBPM would be converted to IF, and digitized by the above commercial board up to 160 MHz sampling rate (Fig.1)[8].

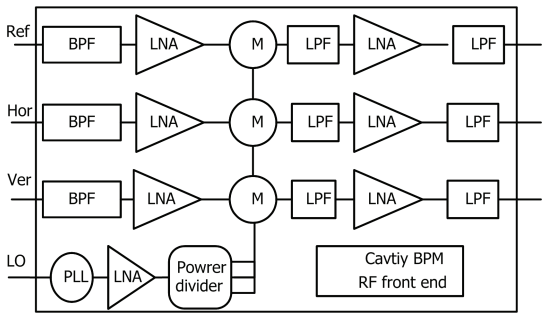

Fig.1 Schematic of RF front end.

The RF signals from CBPM are fed into the first BPF (band pass filter) with the following characteristics: The 4.7-GHz central frequency (5.712 GHz), 100-MHz bandwidth, and 60-dB stop-band attenuation are used to suppress the other harmonics into a low noise amplifier (LNA) with 45-dB gain, to

acquire the broader dynamic range. A mixer with 3.7–7 GHz input bandwidth will process the conversion from RF to IF signal by the high LO power. In the LO channel, an amplifier with high output power of 1-dB compression point is added before the power divider to meet the LO input of the mixer. In the IF section, a 32-MHz bandwidth (11-MHz bandwidth) LPF was used to remove the high order harmonics from the mixer. An IF amplifier accomplishes the last gain adjusting to fulfil the following input requirement of ADCs. The last LPF was used as anti-aliasing filter to suppress other amplified harmonics.

2.2 Front end bunch test

Superior to 1 μm position resolution, the noise level of RF front end and the amplitude stability are less than –70 dBm and 4%, respectively.

In the test process, the power of –100 to –40 dBm was input by using a signal generator and a power divider to generate three-channel RF signals, thus utilizing as the RF front end input power. The output of the RF front end would be sampled by a board ICS1554A-002 with 160-MHz sampling rate. All the data were processed in MATLAB. Fig.2 shows the test diagram, Fig.3 shows the gain line test results.

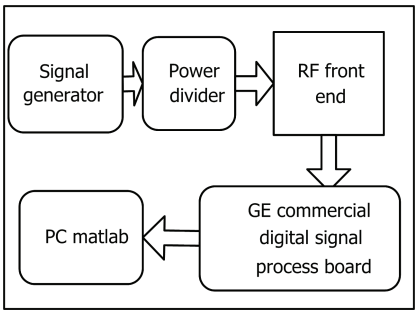

Fig.2 Diagram of RF front end bunch test.

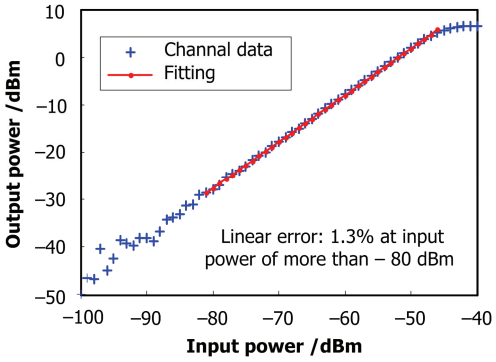

Fig.3 Gain line test of RF front end.

As shown in Fig.4, the linearity error of the three channels is less than 2% at the input power of more than –80 dBm, and the noise level is less than –90 dBm, Amplitude error is less than 0.4% (RMS), achieving the design parameters.

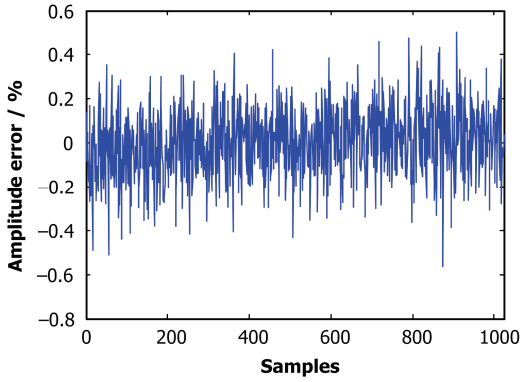

Fig.4 Amplitude error.

3 Algorithm design

In order to tease out the beam position from the skein of the raw CBPM signals, precise demodulations of the amplitudes and phases of the digitized waveforms were needed. In time domain, the output signals were nominally and exponentially decaying sine waves. Two independent methods of fitting and DDC in time-domain processing could accomplish the determination of amplitudes and phases[7,9]. In frequency domain, FFT technique was employed to extract the calibrated amplitudes and phases.

3.1 Fitting

The raw waveform, $V(t)$, of the CBPM output from one channel can be expressed by Eq.(1)[7].

$$V(t)=V_0+Ae^{-0.5t/\tau}\sin[\omega t+\varphi] \quad (1)$$

where A and φ are the amplitude and phase, V_0 is the ADC pedestal value, τ and ω are the decay time constant and angular frequency. When fitting for the A and φ, the τ and ω are fixed, which are determined by fitting using calibration data of the given channel, and their average values are taken as the fixed τ and ω.

3.2 DDC

Also, the CBPM output in time domain is processed by the DDC algorithm, in which the $V(t)$ from a given channel was multiplied by complex LO of the same ω and the raw signal is converted to baseband. A digital

low pass filter, which was used to reduce the high harmonics and noise, was designed by symmetric finite impulse filter (FIR), and implemented by convoluting the complex signal with the certain-coefficient and certain-bandwidth FIR LPF. The demodulated signal can be described in Eq.(2)[1,7].

$$y_{\mathrm{DDC}}(t)=[(y_{\mathrm{digital}}-y_0)\mathrm{e}^{\mathrm{i}\omega_{\mathrm{DDC}}t}]\times\boldsymbol{Filter} \quad (2)$$

where y_{digital} is the raw signal from the ADC, y_0 is the ADC pedestal value, which is determined by taking the mean of the ADC samples before the beam passed through the cavity. ω_{DDC} is the angular frequency equal to the IF from the RF front end. The ***Filter*** is the FIR coefficient vector. The acquired baseband signal peak and its corresponding phase were used to determine beam position and offset direction.

3.3 FFT

Weakening the harmonics influence in time domain, the CBPM signal processing implemented in frequency domain could improve the position resolution. We adopted the FFT technique to demodulate the amplitude. Before FFT, we should use a FIR filter to reduce the harmonics induced by the frequency mixer in RF front end and noise level. Fig.5 shows the diagram of the processing algorithm. As the position of a single pulse in a shot full of micropulses was to be measured, all the algorithms must be implemented on the FPGA device using hardware describe language (HDL). So we only paid attention to the DDC and FFT algorithm.

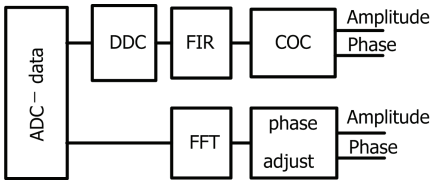

Fig.5 Diagram of the processing algorithm.

4 Bench test

For the systematic performance of signal processing, electronics was evaluated by a dedicated mobile platform using submicron level single step. The newly manufactured cavity was mounted on the platform. A signal generator generated the RF signals, which was input to the cavity by an antenna, then entered to the electronics by the output.

In the test procedure, the RF signal of –16 dBm was input to the antenna. The platform was moved from 0 μm to 100 μm by 2-μm stepping. At every positioning, we acquired 100 samples among which every sample got 256 sampling points[8]. Both fitting and DDC algorithm have equivalent performance[7]. Because the fitting algorithm has much run time, and difficultly implements on an FPGA device, the DDC and FFT algorithm are adopted to demodulate the calibration scale factor and evaluate the position resolution. Also the DDC algorithm, which could be applied in the high/low Q CBPM system, was implemented on the FPGA devices.

4.1 DDC algorithm test

The DDC algorithm was applied to the data sampled by the commercial digitizer, thus obtaining the calibration scale factor (Fig.6).

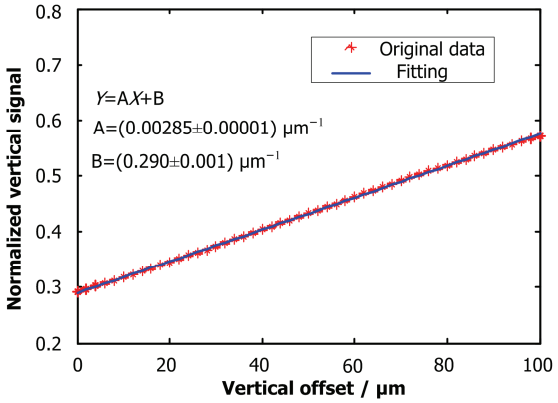

Fig.6 Calibration scale factor of vertical channel.

We positioned the platform at certain offset from the cavity center to match the ADC SNR requirement, and got 1024 samples to evaluate the system position resolution, as shown in Fig.7. We got a resolution of 0.31 μm.

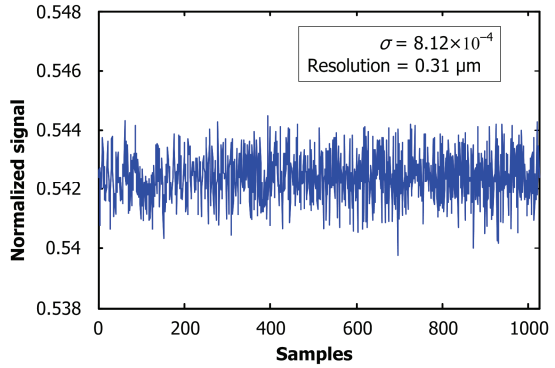

Fig.7 1024 samples at certain offset.

4.2 FFT algorithm test

The same procedure in DDC test was used in FFT test. The calibration scale factor shows that the error bar is smaller in the FFT test than in DDC test (Fig.8).

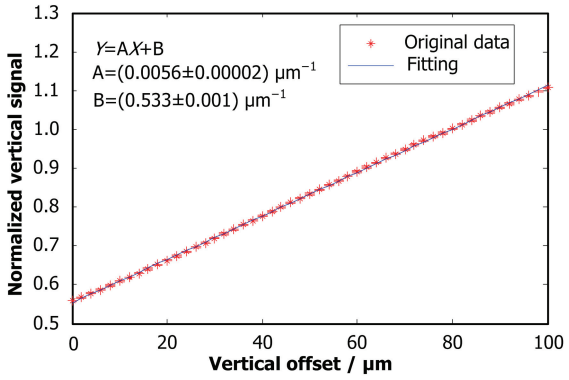

Fig.8 Calibration scale factor using FFT algorithm.

The FFT algorithm reaches the 0.1-μm resolution, as shown in Fig.9.

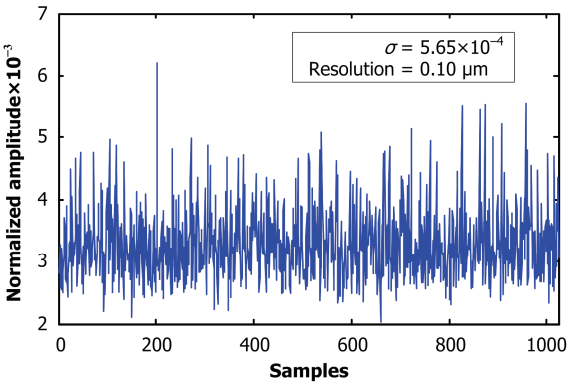

Fig.9 1024 samples at certain offset using FFT algorithm.

4.3 FPGA algorithm test

To meet the measurement of single pulse position, the processing algorithms was implemented on the FPGA device when its function was accomplished using the efficient hardware. Hardware algorithm implemented in a way of parallel operation could improve the processing speed at the cost of hardware resource.

The DDC algorithm on FPGA was implemented by using coordinate rotation digital computer (CORDIC)[10,11], rather than the conventional quadrature-mixing method, in which plenty of RAM resources was used to store the look-up table of sine and cosine by a pair of multipliers. But the CORDIC algorithm could use the shifts and add to perform DDC and coordinate conversion (COC). Also, the pipeline iteration structure makes the system run at high speed. We employ the rotation mode of CORDIC to implement the DDC. The FIR based on Xilinx FIR IP core[12] was used to remove the up-converted component. The demodulation of amplitude and phase in the COC was implemented by using the vectoring mode of CORIDC. Fig.10 shows the architecture of FPGA algorithm.

The same test method was used in FPGA algorithm test. The calibration scale factor was shown in Fig.11. Fig.12 shows that the 0.49-μm resolution is worse in FPGA algorithm than in the DDC algorithm due to the data-bit truncation error.

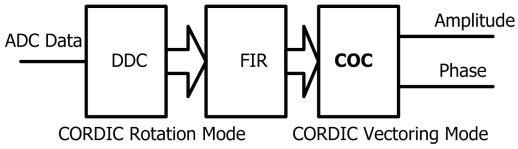

Fig.10 Architecture of FPGA algorithm.

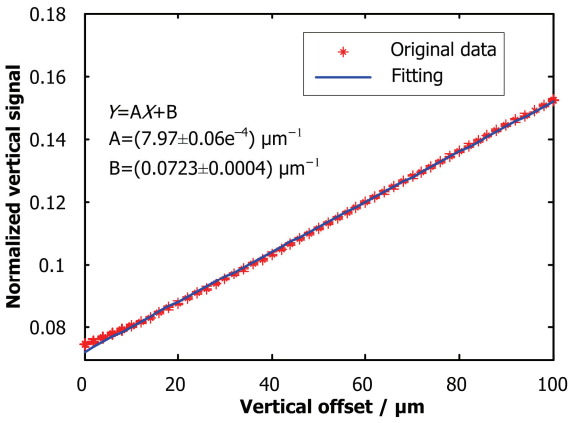

Fig.11 Calibration scale factor in FPGA algorithm.

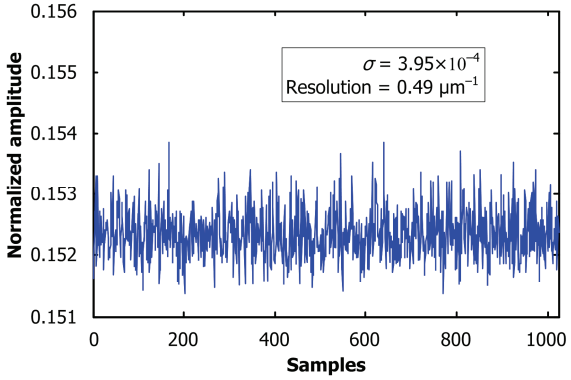

Fig.12 1024 samples at certain offset.

5 Conclusions

In this study, we accomplished the whole CBPM signal processing system. The relevant digital algorithms have been implemented. In the bunch test, we got the 0.31-μm position resolution by DDC algorithm; and 0.10-μm by FFT algorithm at the input power of –16 dBm, thus meeting the beam position diagnostic in Shanghai soft X-ray FEL facility. The preliminary FPGA algorithm was implemented and the bunch test was conducted to get a little worse resolution than digital algorithm. We look forward to the beam test of the whole CBPM system in the future.

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